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Over 100 million frames per second high speed global shutter CMOS image sensor

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Abstract

This paper presents advancement of ultra-high speed (UHS) global shutter CMOS image sensor technology exceeding 100M frames per second (fps). The development of key technologies toward the next generation UHS global shutter CMOS image sensor are overviewed, that includes high density analog memory integration, pixel-wise memory array architecture, and burst correlated double sampling (CDS) operation. By introducing the newly developed signal readout scheme with minimized pixel pulse transitions, a frame period of photo-electrons transit time is achieved. The fabricated chip prototyping a 3D stacked structure achieved 100Mfps with 80 record length and 125Mfps with 40 record length under room temperature without any cooling systems.
Keywords: Burst CMOS image sensor, 3D stacking, analog memory, burst correlated double sampling

1. INTRODUCTION

Time resolution of image sensors is one of the fundamental performances of image sensors. Figure 1 summarizes relationship of performance categories with regards to speed and time resolution of image sensors. For high speed image sensors utilized in high speed video cameras, the time resolution is determined by the frame period(1-6). On the contrary for image sensors utilized in high speed shutter cameras or lock-in detection cameras such as for time of flight range imaging, fluorescence lifetime imaging and etc(7-8), the time resolution is limited by shutter period or pixel modulation period, which can be shorter than the frame period. Both types of sensors have been extensively researched and their time resolution is continuously improving by continuous technological breakthroughs.
Figure 2 shows the speed limiting factors for a typical CMOS image sensor(5). Here, the factor D and E can be eliminated by an introduction of burst CMOS image sensors with on-chip multi-frame memories(4). The factor A: the transit time of photo-electrons is the ultimate limiting factor for the time resolution(9). Image sensors having multiple photo-electron storage nodes connected in parallel to a photodiode (PD) have been researched for both high speed video camera as well as lock-in detection cameras(7-11). Photo-electrons are collected to designated storage node switching one after another by multi collection gate (MCG)(10-11) or lateral electric field modulator(8, 12). Here, the time resolution is determined by the photo-electrons transit time and the switching time of the charge collection storage nodes, respectively. Very high time resolution such as less than 1ns has been obtained by this scheme, however the number of record length is limited. Utilization of multi-aperture system with lateral electric field modulator pixels and coded shutter has been reported to be useful to achieve both very high speed such as 200Mfps and record length equal to the number of apertures(13).
Meanwhile, the 3D chip stacking technology has been a major technology breakthrough in recent image sensor technology with regards to performance improvements and adding more functionalities(14-19). Recently a three layers stacked CMOS image sensor was reported to be useful to improve the speed by adding DRAM on-chip instead of outputting signal at each frame(15). This can be attributed as a digital burst sensor.

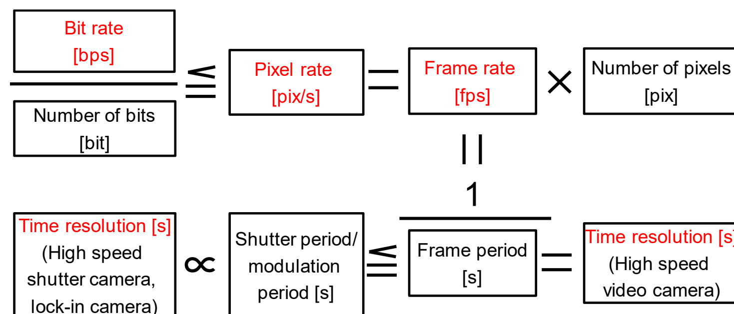

Figure 1. Relationship of performance categories for speed and time resolution of image sensors.

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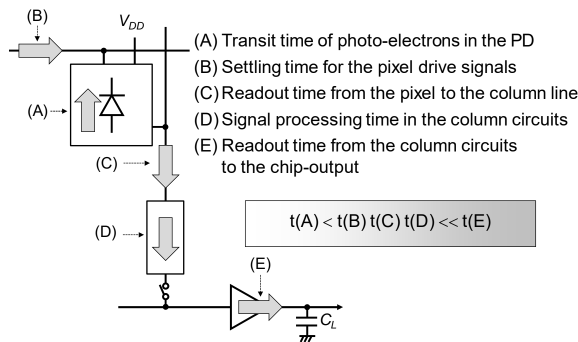

Figure 2. Speed limiting factors of a CMOS image sensor. A frame period equals to the factor A is to be achieved in this work.

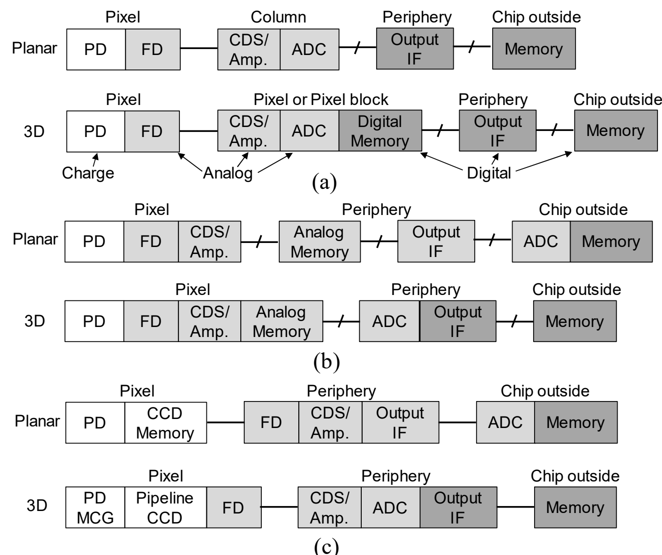

Figure 3. Examples of signal readout chains with planar and 3D stacked structural conditions for (a) digital CMOS image sensors, (b) burst CMOS image sensors with on-chip analog memories and (c) burst CCD image sensors with multi-collection gate (MCG), respectively.

Figure 3(a-c) shows examples of signal readout chains with planar and 3D stacked structural conditions for (a) digital CMOS image sensors[14-19], (b) burst CMOS image sensors with on-chip analog memories[4, 6, 20-26] and (c) burst CCD image sensors with multi-collection gate (MCG)[9-11], respectively. The 3D chip stacking is advantageous for high speed image sensors of these types by means of increasing the parallelism as well as shorting the physical distance of signal readout paths as well as more freedom of metal wiring and so on.
We have developed a burst CMOS image sensors with on-chip analog memories that achieved 1Tpixel/s pixel rate, that is, 10Mfps with 100K pixels and 128 continuous recording length and 20Mfps with 50K pixels and 256 continuous record length[4, 6]. The developed sensors has been utilized in commercialized high speed video camera: HPV-X and HPV-X2 for visualization of various UHS phenomena[20]. There is no high speed cameras currently available yet that supports over 100M fps with long record length such as over 100 with good resolution. This paper presents the advancement and current status of our development on UHS global shutter CMOS image sensor technologies realizing over 100Mfps imaging with large number of pixels and long record length.

2. Over 100Mfps UHS Global Shutter CMOS Image Sensor

2.1 Concept of further performance improvements

Figure 4 shows the schematic illustrations of structures of burst CMOS image sensors with on-chip analog memories, where (a) shows the previously developed planar chip structure with on-chip memories placed on the periphery of pixel array[4, 6], (b) shows an improved structure of (a) with increased number of pixels and record length to be enabled by high density analog memories[21-22], (c) shows a planar structure with pixel-wise analog memory array placed closely each

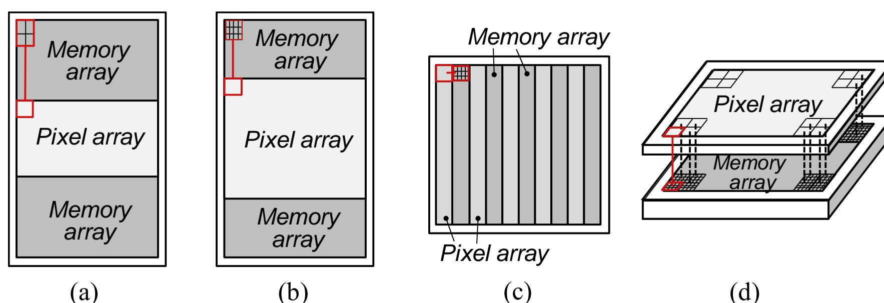

Figure 4. Schematic illustrations of structures of burst CMOS image sensors with on-chip analog memories; (a) the previously developed chip, (b) an improved structure of (a) with high density analog memories, (c) a planar structure with pixel-wise analog memory array placed closely each pixel, and (d) a 3D stacked structure with pixel-wise connections.

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pixel(23-25), and (d) 3D stacked structure with pixel-wise connections for analog memory array placed beneath each light receiving pixel(26). A high density analog memory integration is the primarily important to achieve all of the structures in Figure 4(b-c) with a sufficient number of recording frames. The structure shown in Figure 4(b) is beneficial to increase the number of pixels especially with small pixel pitch as well as to increase the number of analogy memories per pixel. In Figures 4(c) and 4(d), signal wires are much shorter than those of figures 4(a) and 4(b), which is advantageous to increase frame rate as well as to reduce power consumption because the load capacitance to readout signal from pixels to analog memory become much smaller. In the 3D stacked structure shown in Figure 4(d), the light sensitivity is to be improved by an introduction of backside illumination pixel with 100% fill factor. In addition, the number of pixels is more flexibly extended as the chip size is nearly equal to the size of pixel array.

2.2 Developed Key Technologies and Prototype Chip Performances

2.2.1 High Density Analog Memory

The analog memories employed in the previous works are Metal-Oxide-Silicon (MOS) and/or Poly-Si/Oxide/Poly-Si (PIP) capacitors. The capacitance densities of these are typically 4~6 fF/μm^2. The thermal noise arising at the analog memory capacitors is one of the major noise sources in this type of sensor, thus relatively large capacitance value such as about 50fF is suitable. The large capacitance value is also advantageous to maintain signal integrity during signal storing period toward leakage current. DRAM capacitor is most miniaturized capacitor structure, however the leakage current is several order higher than the use of analog signal storage. Consequently, in order to improve the density of analog memory while maintaining low leakage current, we have developed a trench capacitor with improved effective capacitance area(21-22). It utilizes high integrity thermal oxide film and buried poly-Si electrode formed prior to the shallow trench isolation process step. A prototype CMOS image sensor was designed and fabricated having 480 analog memories per pixel as shown in figure 5. By tiling up the set of pixel and analog memory array, a structure shown in figure 4(b) is to be obtained. The layout and cross section diagrams of analog memory is shown in figure 6. The capacitance density of the developed trench capacitor is 30fF/μm^2. Here the signal charge is stored at the poly-Si electrode side, and the counter electrode formed by an inversion layer and n$^+$ region in silicon substrate side is always grounded. In this way, leakage current as well as parasitic light sensitivity due to mixing of photo-induced carriers are suppressed. The developed prototype chip exhibited 10Mfps with 960 record length with half pixel mode(22).

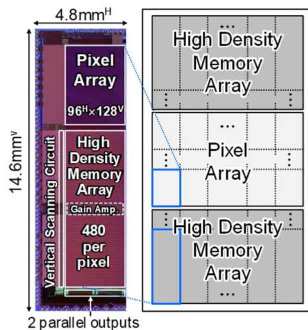

Figure 5. Chip micrograph of a fabricated prototype chip with high density analog memories.

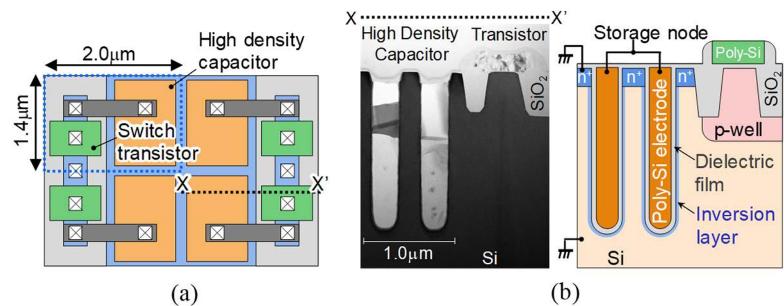

Figure 6. (a) Layout diagram and (b) cross section diagram of the developed analog memory with trench capacitors.

2.2.2 Burst Correlated Double Sampling with Pixel-wise Analog Memory Array

Figure 7 shows the chip micrograph of a fabricated 25^H×100^V planer prototype chip with pixel-wise analog memory array placed closely to each pixel, as illustrated in figure 4(c)(24-25). In order to mimic the 3D stacked structure shown in figure 4(d), the pixel and analog memory array per pixel share a same effective area. Figure 8 shows the pixel circuit diagram of the fabricated chip. The pixel comprises of a high speed charge collection photodiode (PD)(27) directly connected to floating diffusion (FD) which converts photoelectrons to signal voltage, reset gate, the 1st source follower circuit to readout floating diffusion voltage signal, an in-pixel corrected double sampling (CDS) circuit and the 2nd source follower circuit, switches to select or bypass the in-pixel CDS circuit, and a 4^H×20^V analog memories and its memory addressing and readout circuits. The analog memory employs conventional MOS capacitors. The number of analog memories would increase to over 300 when the trench capacitor was used. The signal output wire length is about 40μm. Compared to our previous chip having the signal output wire length of about 8mm it is an over two-digit reduction. Figure 9(a-b) shows the pixel pulse timing diagram of the burst corrected double sampling operation and the potential diagram of PD and FD for electrons, respectively(25). The built-in potential gradient or electric field of about 500V/cm is formed in fully depleted PD region by means

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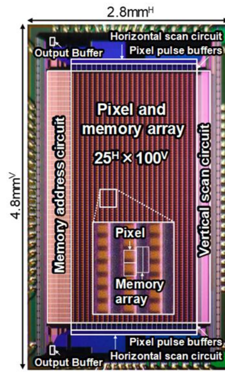

Figure 7. Chip micrograph of a fabricated prototype chip with pixel-wise analog memory array.

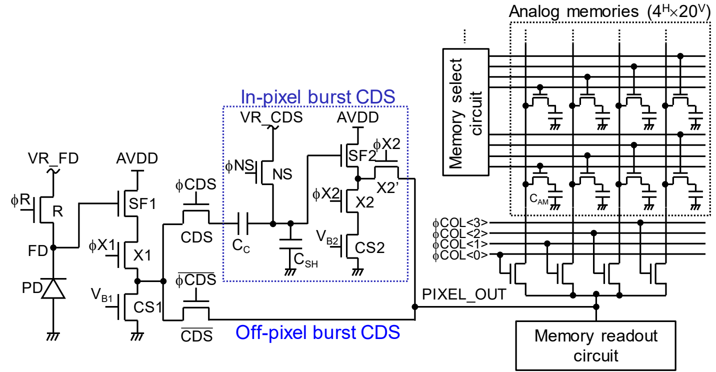

Figure 8. Circuit schematic diagram of pixel and analog memory array.

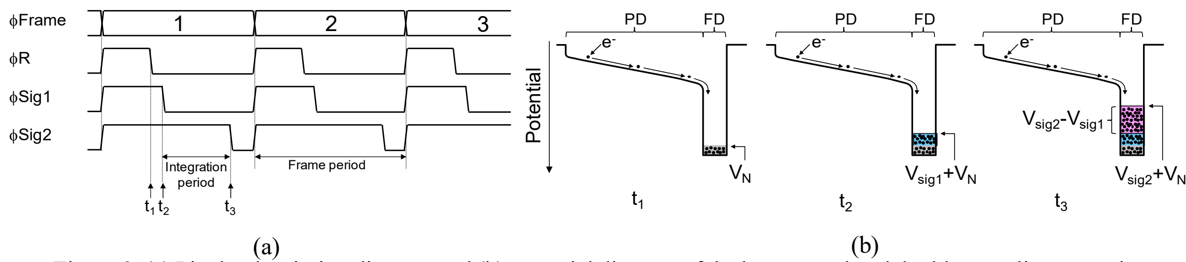

Figure 9. (a) Pixel pulse timing diagram and (b) potential diagram of the burst correlated double sampling operation.

of dopant concentration difference as well as the control of width of buried n-type layer[27]. The PD size is $21.3^H \times 30.0^V \mu m^2$. A transfer gate can be physically inserted like a conventional 4T-pixel CMOS image sensor, however for the burst CDS operation, the potential barrier of transfer gate from PD to FD should be removed by the control of gate bias condition during this operation. The photoelectron transit time of this PD has been verified to be about 5ns by experiments[27]. Here, the potential top of FD is directly connected to the potential bottom of the PD. In this way, photoelectrons are always flowing toward FD. After resetting the PD and FD at t_1, the thermal noise (V_N) is remained at FD. Right after t_1, the first signal voltage V_{sig1} comprised of V_N and light signal due to photoelectrons coming to FD during t_2-t_1 is readout at t_2. Then, after the integration period: t_3-t_2, the second signal voltage V_{sig2} comprised of V_N and light signal due to photoelectrons during t_3-t_1 is readout at t_3. By subtracting V_{sig1} from V_{sig2} at the in-pixel CDS circuit or off-pixel after reading out memory signals, light signal during the integration period t_3-t_2 is obtained. Here, the integration period is so short such as less than 1μs for high speed imaging usage, the thermal noise at FD as well as the threshold voltage variation of SF driver are removed just like a general CDS operation. In this way, very high speed framerate equal to the photoelectron transit time in PD is to be achieved. The number of signal readout after resetting phase can be more than twice unless the FD is oversaturated.

Figure 10 shows the current consumption per pixel for the previous work[6] and this work with in-pixel burst CDS mode at 100Mfps and off-pixel burst CDS mode at 125Mfps, respectively. In this work, the third source follower buffer (SF3) which is placed in-between the pixel array and memory array is eliminated as well as, the current values of SF1 and SF2 are reduced. Consequently the current consumption per pixel is significantly reduced compared to the previous work even though the framerate is improved, such as less than 1/4 of current even at over 6 times higher frame rate in the case of off-pixel burst CDS operation mode.

Figure 11 shows the imaging shooting experimental setup and the sample images of a rotating object captured at 25Mfps with in-pixel burst CDS mode and 125Mfps with off-pixel burst CDS mode, respectively. High quality images were successfully obtained at 125Mfps without any cooling systems.

Table I shows the performance summary of the developed prototype chip. The process technology is based on 0.18μm 1-poly-Si, 5-metal layer technology for both of the chips shown in this paper.

Figure 12 shows a maximum frame rate as a function of record length to benchmark the developed prototype chip in this work with recently reported burst image sensors. Over 100Mfps imaging results with up to 80 record length are demonstrated in this work. The record length is to be further improved when the developed trench capacitor is employed for analog memory of this chip structure.

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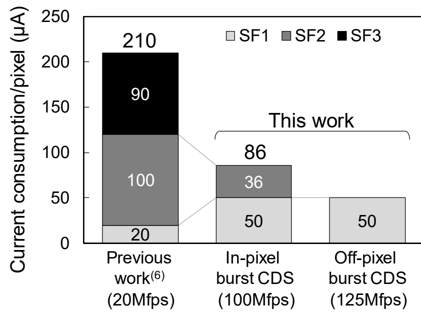

Figure 10. Current consumption of the previous chip and the fabricated prototype chip in this work.

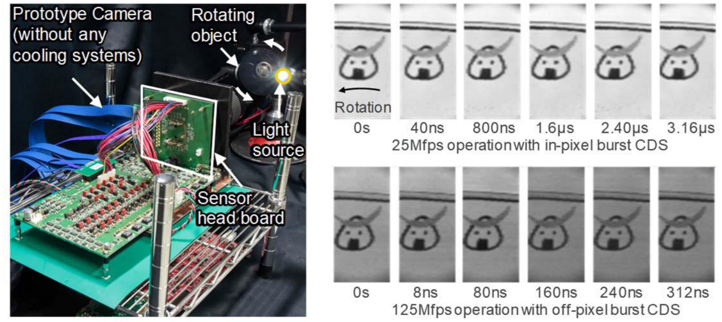

Figure 11. Image shooting setup and sample images captured at 25Mfps and 125Mfps with in-pixel and off-pixel burst CDS operations, respectively.

Table I
Performance summary of prototype chip with pixel-wise analog memory and burst CDS operation.

Technology	1P5M 0.18μm CMOS	
Supply voltage [V]	3.3	
Pixel pitch [μm] (3D stacking equivalent)	$69.12^H \times 34.56^V$ ($34.56^H \times 34.56^V$)	
Photodiode size [μm^2]	$30.00^H \times 21.34^V$	
# of pixels	$25^H \times 100^V$	
# of analog memories /pixel	80	
Maximum frame rate [Mfps]	In-pixel burst CDS mode	Off-pixel burst CDS mode
	100	125
Record length	80	40

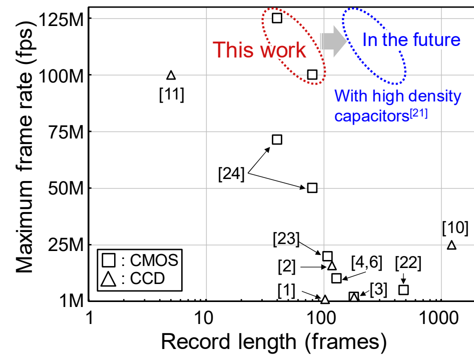

Figure 12. Comparison of the maximum frame rate as a function of record length for the prototype chip and recently reported burst image sensors.

3. CONCLUSIONS

In this paper, key technologies for the next generation UHS CMOS image sensors were presented, including high density analog memory integration using trench capacitors with 30fF/μm^2, pixel-wise memory array architecture with fully pixel parallel and short signal path, and the burst CDS readout operation with minimized pulse transitions. The prototype chip with pixel-wise memory array mimicking the 3D stacked chip architecture achieved the frame period of photo-electrons transit time in PD, and exhibited 100Mfps with 80 record length with on-chip burst CDS operation and 125Mfps with 40 record length with off-chip burst CDS operation, respectively. Moreover, the current consumption per pixel was reduced to less than 1/4 at over 6 times higher frame rate compared to the previous work, i.e., the developed technology is scalable to larger number of pixels. Consequently, the obtained results are promising for achieving over 100Mfps CMOS image sensor with high resolution and long record length.

REFERENCES

[1] T. Goji Etoh, D. Poggemann, A. Ruckelshausen, A. Theuwissen, G. Kreider, H.-O. Folkerts, "A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of 103 Frames," *2002 IEEE International Solid-State Circuits Conference*, *Dig. Tech. Papers*, 46-47 (2002).

[2] T. G. Etoh, D. H. Nguyen, S. V. T. Dao, C. L. Vo, M. Tanaka, K. Takehara, T. Okinaka, H.V. Kuijk, W. Klassens, J. Bosiers, M. Lasser, D. Ouellette, H. Maruyama, T. Hayashida and T. Arai, "A 16 Mfps 165 kpixel backside-illuminated CCD," *IEEE Intl. Solid-State Circ. Conf., Dig. Tech.*, 406-407 (2011).

[3] J. Crooks, B. Marsh, R. Turchetta, K. Taylor, W. Chan, A. Lahav, A. Fenigstein, "Kirana: A solid-state megapixel uCMOS image sensor for ultra-high speed imaging," *Proc. IS&T/SPIE Electronic Imaging, 8659*, 865903-1-14 (2013).

[4] Y. Tochigi, K. Hanzawa, Y. Kato, R. Kuroda, H. Mutoh, R. Hirose, H. Tominaga, K. Takubo, Y. Kondo, S. Sugawa, "A Global-Shutter CMOS Image Sensor With Readout Speed of 1-Tpixel/s Burst and 780-Mpixel/s Continuous," *IEEE J. Solid-State Circuits,* 48, 329-338 (2013).

[5] S. Sugawa, "Ultra-High Speed Imaging," *IEEE Intl. Solid-State Circ. Conf., Forum, Scientific Imaging* (2013).

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[6] R. Kuroda, Y. Tochigi, K. Miyauchi, T. Takeda, H. Sugo, F. Shao and S. Sugawa, "A 20Mfps Global Shutter CMOS Image Sensor with Improved Light Sensitivity and Power Consumption Performances," *ITE Trans. on MTA,* 4, 149-154 (2016).
[7] Cyrus S. Bamji, Swati Mehta, Barry Thompson, Tamer Elkhatib, Stefan Wurster, Onur Akkaya et al., "1Mpixel 65nm BSI 320MHz Demodulated TOF Image Sensor with 3.5µm Global Shutter Pixels and Analog Binning," *2018 IEEE International Solid-State Circuits Conference, Tech. Dig. Papers*, 94-95 (2018).
[8] Min-Woong Seo , Yuya Shirakawa, Yoshimasa Kawata, Keiichiro Kagawa, Keita Yasutomi, and Shoji Kawahito, "A Time-Resolved Four-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy," *IEEE Journal of Solid-State Circuits*, 53, 8, 2319-2330 (2018).
[9] Takeharu Goji Etoh, Anh Quang Nguyen, Yoshinari Kamakura, Kazuhiro Shimonomura, Thi Yen Le and Nobuya Mori, "The Theoretical Highest Frame Rate of Silicon Image Sensors," *SENSORS*, 17, 3, 483-1-15 (2017).
[10] Vu Truong Son Dao, Nguyen Ngo, Anh Quang Nguyen, Kazuhiro Morimoto, Kazuhiro Shimonomura, Paul Goetschalckx, "An Image Signal Accumulation Multi-Collection-Gate Image Sensor Operating at 25 Mfps with 32×32 Pixels and 1220 In-Pixel Frame Memory," *SENSORS*, 18, 9, 3112-1-11 (2018).
[11] T. G. Etoh, K. Shimonomura, Q. A. Quang, Kosei Takehara, Yoshinari Kamakura, Paul Goetschalckx, Luc Haspeslagh, "A 100 Mfps image sensor for biological applications," *SPIE Photonics West 2018* (2018).
[12] S. Kawahito, G. Baek, Z. Li, S.-M. Han, M-W Seo, K. Yasutomi, K. Kagawa, "CMOS Lock-in Pixel Image Sensors with Lateral Eelectric Field Cotrol for Time-Resolved Imaging", *Proc. 2013 International Image Sensor Workshop*, 361-364 (2013).
[13] F. Mochizuki, K. Kagawa, S-I. Okihara, W-M. Seo, B. Zhang, T. Takasawa, K. Yasutomi, S. Kawahito, "Single-Shot 200Mfps 5×3-Aperture Compressive CMOS Imager," *2015 IEEE International Solid-State Circuits Conference, Dig. Tech. Papers*, 116-117 (2015).
[14] Shunichi Sukegawa, Taku Umebayashi, Tsutomu Nakajima, Hiroshi Kawanobe, Ken Koseki, Isao Hirota, "A 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor," *2013 IEEE International Solid-State Circuits Conference, Dig. Tech. Papers*, 484-485 (2013).
[15] Tsutomu Haruta, Tsutomu Nakajima, Jun Hashizume, Taku Umebayashi, Hiroshi Takahashi, Kazuo Taniguchi et al., "A 1/2.3inch 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM," *2017 IEEE International Solid-State Circuits Conference, Dig. Tech. Papers*, 76-77 (2017).
[16] Hidetake Sugo, Shunichi Wakashima, Rihito Kuroda, Yuichiro Yamashita, Hirofumi Sumi, Tzu-Jui Wang, Po-Sheng Chou, Ming -Chieh Hsu and Shigetoshi Sugawa, "A Dead-time Free Global Shutter CMOS Image Sensor with in-pixel LOFIC and ADC using Pixel-wise Connections," *2016 Symposium on VLSI Circuits, Tech. Dig.*, 224-225 (2016).
[17] Toshiki Arai, Toshio Yasue, Kazuya Kitamura, Hiroshi Shimamoto, Tomohiko Kosugi, Sung-Wook Jun et al., "A 1.1-µm 33-Mpixel 240-fps 3-D-Stacked CMOS Image Sensor With Three-Stage Cyclic-Cyclic-SAR Analog-to-Digital Converters," *IEEE Transactions on Electron Devices*, 64, 12, 4992-5000 (2017).
[18] Tomohiro Takahashi, Yuichi Kaji, Yasunori Tsukuda, Shinichiro Futami, Katsuhiko Hanzawa, Takahito Yamauchi et al., "A Stacked CMOS Image Sensor With Array-Parallel ADC Architecture," *IEEE Journal of Solid-State Circuits*, 53, 4, 1061-1070 (2018).
[19] Masaki Sakakibara, Koji Ogawa, Shin Sakai, Yasuhisa Tochigi, Katsumi Honda, Hidekazu Kikuchi et al., "A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC," *2018 IEEE International Solid-State Circuits Conference, Dig. Tech. Papers*, 80-81 (2018).
[20] Rihito Kuroda and Shigetoshi Sugawa, "Cameras with On-chip Memory CMOS Image Sensors," *The Micro-World Observed by Ultra High-Speed Cameras*, Springer, 103-124 (2018).
[21] Manabu Suzuki, Masashi Suzuki, Rihito Kuroda, Yuki Kumagai, Akira Chiba, Noriyuki Miura, Naoya Kuriyama, Shigetoshi Sugawa, "An Over 1Mfps Global Shutter CMOS Image Sensor with 480 Frame Storage Using Vertical Analog Memory Integration," *International Electron Devices Meeting, Tech. Dig.*, 212-215 (2016).
[22] Manabu Suzuki, Masashi Suzuki, Rihito Kuroda, Yuki Kumagai, Akira Chiba, Noriyuki Miura, Naoya Kuriyama, Shigetoshi Sugawa, "10Mfps 960 Frames Video Capturing Using a UHS Global Shutter CMOS Image Sensor with High Density Analog Memories," *Proc. 2017 International Image Sensor Workshop*, 308-311, 2017.
[23] L. Wu, D. San Segundo Bello, P. Coppejans, J. Craninckx, P. Wambacq, J. Borremans, "A 20 Mfps high frame-depth CMOS burst-mode imager with low power in-pixel NMOS-only passive amplifier," *Proc. of SPIE*, 10328, 1032803-1-6 (2016).
[24] Manabu Suzuki, Masashi Suzuki, Rihito Kuroda, Shigetoshi Sugawa, "A Preliminary Chip Evaluation toward Over 50Mfps Burst Global Shutter Stacked CMOS Image Sensor," *IS&T International Symposium on Electronic Imaging 2018*, 398-1-4 (2018).
[25] M. Suzuki, R. Kuroda and S. Sugawa, "A 125Mfps Global Shutter CMOS Image Sensor with Burst Correlated Double Sampling during Photo-Electrons Collection," *Extended Abstracts of 2018 International Conference on Solid State Devices and Materials*, 593-594 (2018).
[26] Philippe Martin-Gonthier, Fernando Raymundo, Pierre Magnan, "High-density 3D interconnects Technology: The key for burst-mode very high speed imaging?," *Proc. 2015 International Image Sensor Workshop*, 142-145, 2015.
[27] K. Miyauchi, T. Takeda, K. Hanzawa, Y. Tochigi, S. Sakai, R. Kuroda, H. Tominaga, R. Hirose, K. Takubo, Y. Kondo and S. Sugawa, "Pixel Structure with 10 nsec Fully Charge Transfer Time for the 20M Frame Per Second Burst CMOS Image Sensor," *Proc. IS&T/SPIE Electronic Imaging,* 9022, 902203-1-12 (2014).

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