A 20Mfps Global Shutter CMOS Image Sensor with Improved Sensitivity and Power Consumption

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ABSTRACT

In this work, a 20 Mfps global shutter CMOS image sensor with improved sensitivity and power consumption is demonstrated. Due to the process technology development and the improvement of single readout circuitry with decreased supply voltage, the fill factor, the conversion gain and the readout gain were all improved from the previous chip and eight times higher light sensitivity and 50 % decrease of power consumption were achieved simultaneously. The impact of the performance improvements was confirmed to be significant based on the captured images of UHS phenomena.

INTRODUCTION

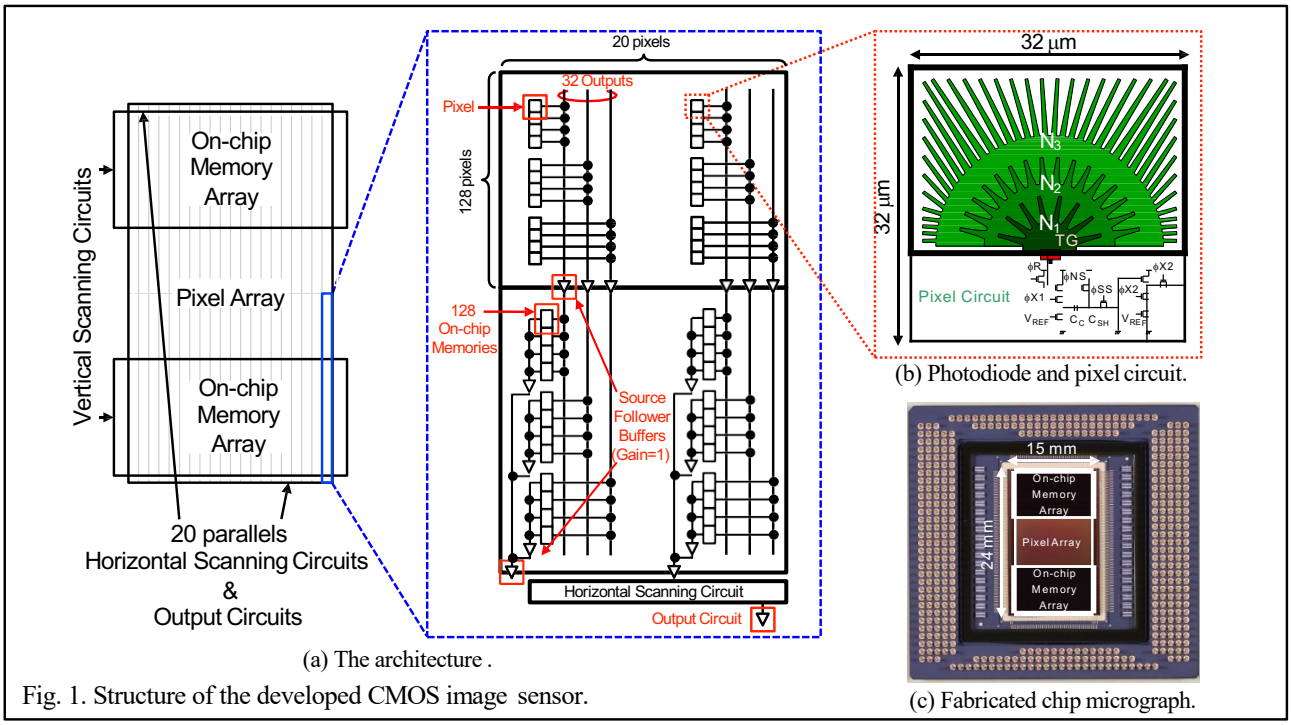
Ultra high speed (UHS) imaging technologies are now being utilized in various scientific and engineering fields to reveal and analyze what has not been seen before [1]. We have developed architecture for global shutter UHS CMOS image sensor with multiple on-chip analog memories per pixel [2]. The previously developed UHS CMOS image sensor has simultaneously achieved 10 Mfps, 10 Kpixels, 128 frames. In UHS imaging, sensitivity and power consumption are the major stumbling blocks to be overcome in order to improve the sensor performance to the next level. In this work, a newly developed UHS CMOS image sensor is demonstrated that achieves eight time higher sensitivity and 50 % power consumption reduction simultaneously.

DEVELOPED SENSOR CHIP AND MEASUREMENT RESULTS

A new UHS CMOS image sensor was developed in this work under the condition that the optical format, the pixel pitch and the pin-assignment are to be the same as those of previous sensor chip in order to fairly verify the effect of introduced technologies on sensitivity and power consumption. The basic structure of developed UHS CMOS image sensor that contains pixel region and frame memory region is similar to those of frame transfer CCD and CMOS image sensors [3-4]. By an introduction of several key technologies such as high speed charge collection PD, multiple pixel column output lines, in-pixel CDS circuit and current sources, the developed UHS CMOS image sensor achieves signal reading out from the pixel region to the on-chip memory region within 10 ns at each frame. The image signals are stored in on-chip memories and readout after the end of video capturing. Consequently, a burst video capturing over 10 Mfps is achieved. In the UHS CMOS image sensor in this work, a higher light sensitivity is to be achieved by the following three means; increasing number of incident photons under a same light illumination by increasing the fill factor, increasing conversion gain by reducing the floating diffusion capacitance enabled by optimization of PD's buried n-layer, and increasing of signal readout gain by improving the readout circuit. Also, lower power consumption is to be achieved by a decrease of power supply voltage from 5.0 V to 3.3 V.

Fig.1 (a) and (b) show the block diagram and the pixel circuit including photodiode structure of the developed sensor in this work. The numbers of pixels and on-chip memories, the positions of PADs and the chip package were completely the same as those of the previous chip. It is beneficial for an easy substitution of the image sensor chips of the formerly developed UHS video cameras.

The chip fabrication process technology was completely renewed from the previous one regarding both FEOL and BEOL processes. As a result, the fill factor was improved by using a more miniaturized 6M technology instead of previous 5M one. The PD structure achieving 20 Mfps full charge transfer for the large area PD was developed [5]. By generating an electric field in PD greater than 400 V/cm toward the FD using three levels of dopant concentration and shape control of the buried n-layer, a high conversion gain is to be obtained by forming small capacitance FD on the edge of PD. Also, the PD junction formation process was optimized to enhance the QE especially for UV-light waveband [6]. Moreover, analog memory capacitance was increased by developing a high area efficiency capacitor, resulting in an improvement of the signal readout gain from analog memory to the signal line. In addition to that, the power supply voltage was decreased from previous 5.0 V to 3.3 V and voltage transfer range of signal readout chain was re-designed so that the FWC is maintained while decreasing the



(a) The architecture .

(b) Photodiode and pixel circuit.

(c) Fabricated chip micrograph.

Fig. 1. Structure of the developed CMOS image sensor.

power consumption. Fig.1 (c) shows the fabricated chip micrograph.

Fig.2 shows the photoelectric conversion characteristic. A input-referred temporal noise was about 5 e^- and an input-referred FWC of 10000 e^- was obtained. Fig.3 shows the output referred spectral sensitivity characteristics of the developed sensor in this work and previous one. About eight-times improvement was confirmed at the wavelength of around 550 nm. Also, the spectral sensitivity range is extended to UV-light waveband for the developed sensor in this work. This is beneficial to capture ultra-high speed phenomenon with UV-light, such as to capture dynamic behavior of plasma and flame. Fig.4 shows the characteristic of image lag. In this experiment, the incident light from 635 nm LD was cut off right before the frame number 0, the output signal at frame number 1 and more were at the dark level, indicating the image lag was under the detection limit even at 20Mfps operation. Fig.5 shows the chip temperature behavior during 10Mfps operation with full pixel mode without a cooling system. The chip temperature was under 50 even after 60 sec operation time. Fig. 6 shows the power consumption of the developed sensor in this work at various frame rate with full pixel and half pixel modes. Due to the reduction of the power supply voltage, the power consumption at 1Tpixe/sec operation was reduced by half, i.e., 10 W compared to 20 W of the previous chip. The performances of the developed UHS CMOS image sensor are summarized in Table 1.

Figs.7 and 8 shows the sample images captured by the developed sensor chip in this work and previous one, respectively. The effectiveness of sensitivity improvement is clearly recognized by the higher SNR images captured by the developed sensor in this work. High sensitivity is to be greatly useful for capturing microscopic UHS phenomenon, capturing images with a deeper depth of focus, and capturing light emitting objects.

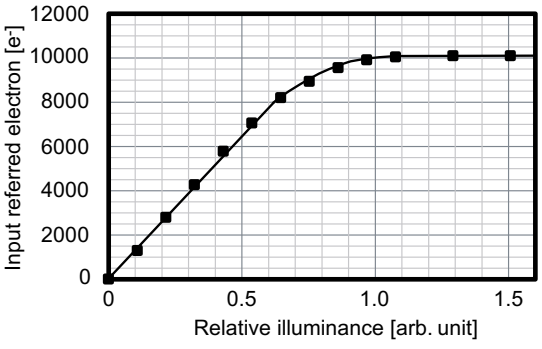


Fig. 2. Photoelectric conversion characteristics.

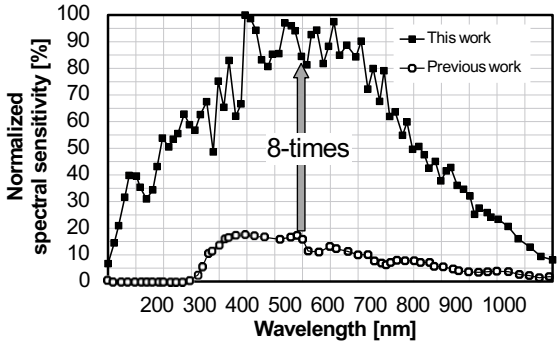


Fig. 3. Spectral sensitivity characteristic.

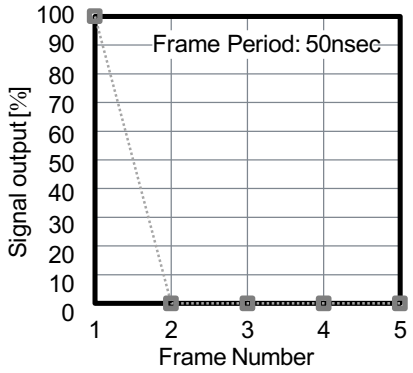


Fig. 4. Image lag characteristic.

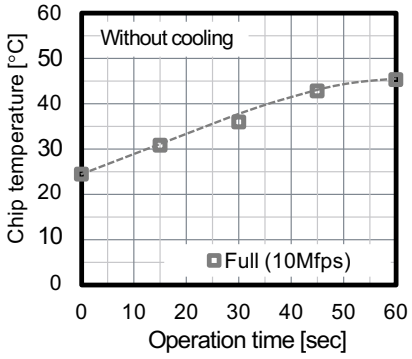


Fig. 5. Chip temperature as a function of operation time with 10Mfps.

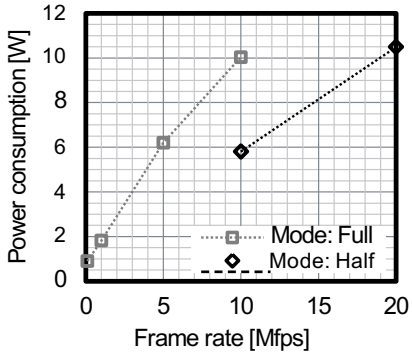


Fig. 6. Power consumption as a function and frame rate.

CONCLUSION

Eight times sensitivity improvement and 50 % reduction of power consumption of UHS CMOS image sensor were successfully achieved by improving pixel level light sensitivity and signal readout gain while decreasing the power supply voltage from 5V to 3.3V. The effectiveness of the performance improvement was confirmed to be significant based on the captured images of UHS phenomena.

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Table 1 Summary of the developed image sensor performance.

Technology		1P6M 0.18μm CMOS with Pinned Photodiode			
Die Size		$15mm^H \times 24mm^V$			
Pixel Size, Photodiode Size		$32\mu m^H \times 32\mu m^V$, $30.00\mu m^H \times 21.34\mu m$			
# of Pixels	Total, Effective	$400^H \times 256^V$, $400^H \times 250^V$			
Aperture Ratio		55%			
# of Parallel Outputs		40			
# of PADs		424			
# of frames in Burst Operation		Full	128	Half	256
Maximum Frame Rate (Read-out speed)	Burst		10Mfps (1Tpixel/s)		20Mfps (1Tpixel/s)
	Continuous		7.8kfps (780Mpixel/s)		15kfps (780Mpixel/s)
Conversion Gain (Input Referred)		112μV/e-			
Full Well Capacity		10,000e-			
Power Consumption		10W @ 1Tpixel/s			
Image Lag @ 20Mfps		below the measurement limit			
Spectral Sensitive Range (Relative Sensitivity ≥ 10% of the peak)		200nm - 1000nm			
Full Charge Transfer Time		≤ 10nsec			

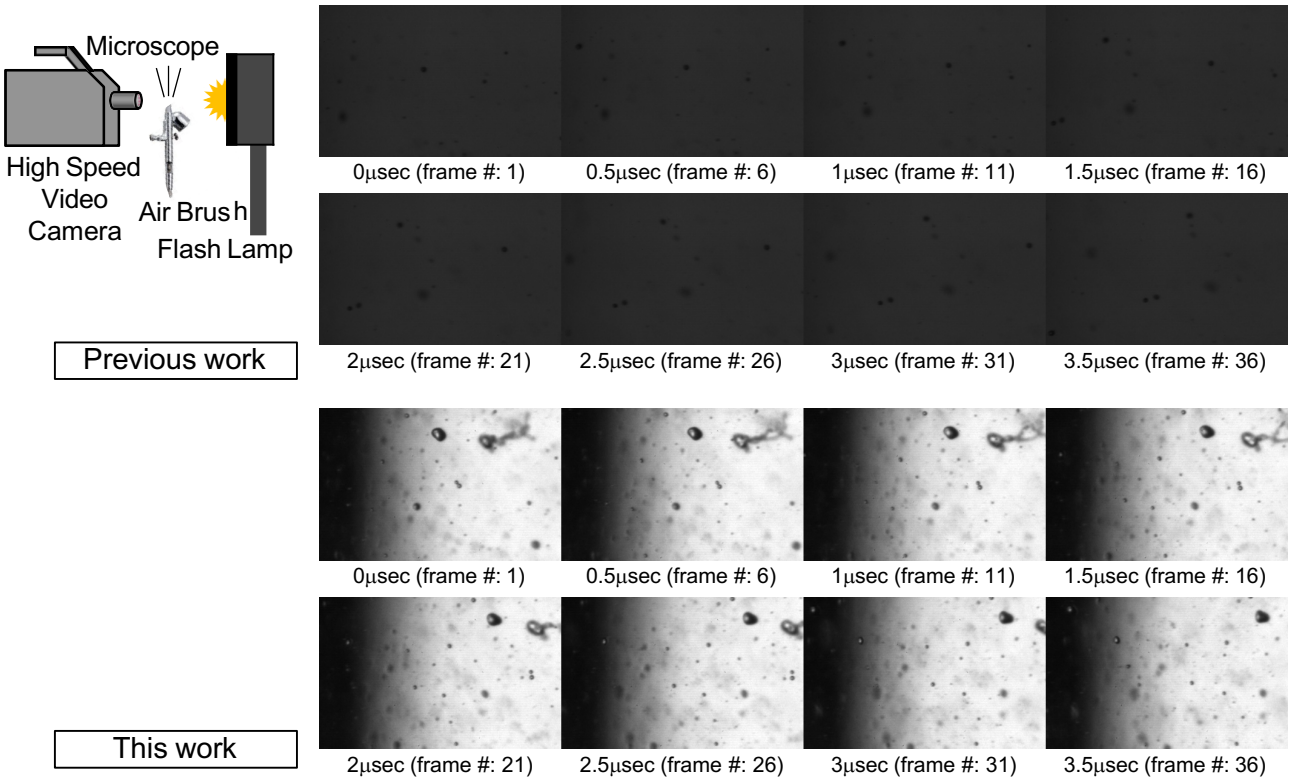

Fig. 7. Sample images of water mist injected from an air brush taken at 10M fps burst half resolution video operation. Upper: images taken by the previously developed sensor chip [1]. Lower: image taken by the developed sensor chip this work.

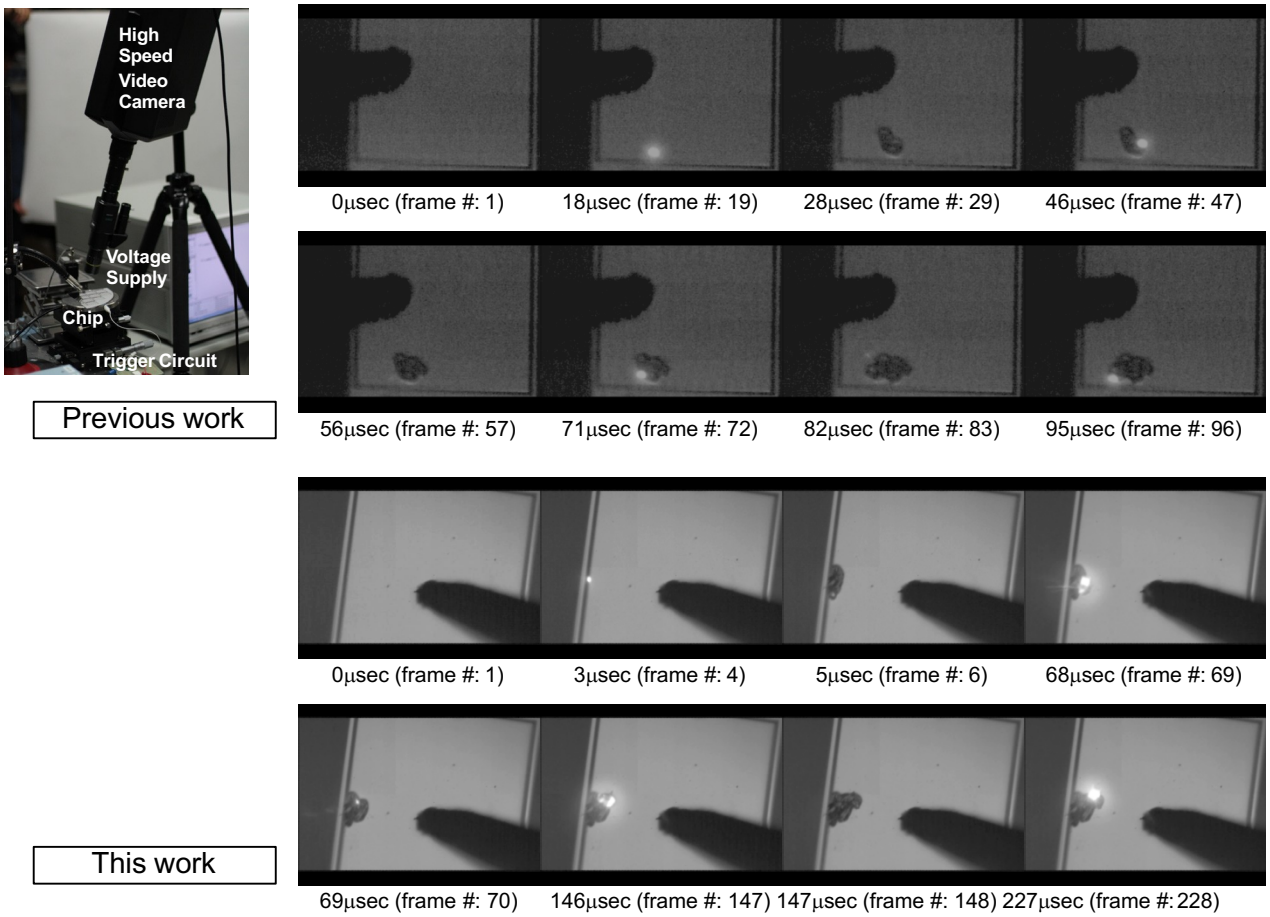

Fig. 8. Sample images of the electric field breakdown in Al/SiO_2(100nm)/n-Si MOS capacitor taken at 1M fps burst half resolution video operation. Upper: images taken by the previously developed sensor chip [1]. Lower: image taken by the developed sensor chip this work.